

Please amend Claim 1 as follows:

1. (AMENDED) A method of forming self-aligned, anti-via
interconnects in an integrated circuit device comprising:
providing a semiconductor substrate;
depositing a metal layer overlying said semiconductor
5 substrate;
etching through said metal layer to form connective
lines;
thereafter etching partially through said metal layer
to form vias;
10 thereafter depositing a dielectric layer overlying
said vias, said connective lines and said semiconductor
substrate; and
polishing down said dielectric layer to complete said
self-aligned, anti-via interconnects in the manufacture of
15 the integrated circuit device.

Please amend Claim 9 as follows:

9. (AMENDED) A method of forming self-aligned, anti-via
interconnects in an integrated circuit device comprising:
providing a semiconductor substrate;

depositing a first metal layer overlying said
5 semiconductor substrate;
depositing a second metal layer overlying said first
metal layer;
depositing an anti-reflective coating layer comprising
titanium nitride (TiN) overlying said second metal layer;
10 etching through said anti-reflective coating layer,
said second metal layer, and said first metal layer to form
connective lines;
thereafter etching through said anti-reflective
coating layer and said second metal layer to form vias;
15 thereafter depositing a dielectric layer overlying
said vias, said connective lines and said semiconductor
substrate; and
polishing down said dielectric layer to complete said
self-aligned, anti-via interconnects in the manufacture of
20 the integrated circuit device wherein said anti-reflective
coating layer is a polishing stop.

REMARKS